METHOD FOR IP CHARACTERIZATION AND PATH FINDING, AND COMPUTER READABLE RECORDING MEDIUM FOR STORING PROGRAM THEREOF

DESCRIPTION

BACKGROUND OF THE INVENTION

[Para 1]   Field of the Invention

[Para 2]   The present invention relates to a method applied in Electronic Design Automation (EDA), and more particularly, to a method for Intellectual Property (IP) component characterization and a method for path finding thereof.

[Para 3]   Description of Related Art

[Para 4]   Thanks to technology progress in computer science, electronics industry is rapidly growing now. For example, Electronic Design Automation (EDA) is a technique, which assists the development engineers to design and simulate the electronic circuitry by using the computing power of the computer system. Especially in developing the Integrated Circuit (IC), different kinds of automation tools had played a significant role in the works such as function verification, layout, electricity analysis, and IC simulation.

[Para 5]   In addition, in order to follow the right trend of intensive circuitry and fulfill the requirement of reducing the product development time, how to develop a most economical chip product has become a major topic for development engineers now, and reusing of the circuitry design is one of the techniques to achieve this object. In other words, by applying this technique, various functional circuitries which are well designed layout can be repeatedly used to build up a new Application Specific Integrated Circuit (ASIC). Therefore, the development process of the IC product can be completed in a

very short time period. Here, the well designed circuitry layout that can be repeatedly used is also known as an IP (Intellectual Property) component.

[Para 6] In general, an estimate data related to the IP component characteristic can be obtained at the same time when the IP component is being obtained. For instance, the information such as the maximum power consumption and the maximum delay time can be obtained from the developer designing the IP component. However, both of the electrical energy consumed in the circuitry and the delay time it outputs are varied based on different input. When using the IP component, the estimate data of the IP component provided originally is not good enough to accurately provide information related to its operating characteristic.

[Para 7] In the prior art, various test data are determined and provided by development engineers based on their own professional knowledge and working experience, and the test data are sequentially and manually input into the system with the help of a simulation program so as to obtain a report corresponding to each of the simulation results. Then, the key values (e.g. timing, power, etc.) it requires are manually extracted from the report of the simulation results, and the extracted key values are manually keyed in to generate an IP characteristic library which is used by subsequent development process. However, the paths in the IP component are very complicated, thus it is not feasible to manually determine test data for all paths in the IP component. Furthermore, for considering time efficiency, in the method of manually inputting the test data and cooperating with the simulation software to obtain the IP characteristic library, it is possible that only part of the test data are selected for simulation based on the physical requirements and the developer's experience, thus a complete IP characteristic library cannot be obtained.

SUMMARY OF THE INVENTION

[Para 8] Therefore, the present invention is directed to a method of IP characterization which can automatically test characteristics of all paths in the IP component so as to generate a complete IP characteristic library.

[Para 9]   The present invention is directed to a method of finding path in IP component which can automatically find all paths in the IP component.

[Para 10]   The present invention is directed to a computer readable recording media for storing program.

[Para 11]   According to an embodiment of the present invention, first, an Intellectual Property (IP) component is provided. Then, a plurality of test patterns for all paths in the IP component is automatically generated. The test patterns are sequentially input into the IP component for simulation, and a plurality of corresponding simulation results is generated. Finally, an IP characteristic library is generated based on the simulation results.

[Para 12]   According to an embodiment of the present invention, the step of automatically generating the plurality of test patterns for all paths in the IP component comprises: automatically finding all paths in the IP component; and generating a corresponding test pattern for each path.

[Para 13]   The present invention is also directed to a method of finding paths in IP component. First, an Intellectual Property (IP) component is provided. Then, an ESD path is identified and excluded. If there is a path point, which was not previously searched, the path point is selected. Then, it is determined whether or not one path among the multiple paths of the selected path point has reached the end point of the path. A next path point, which is connected by the path of the selected path point is then searched by selecting a connection terminal of a transistor based on the transistor rule. In addition, a next path point, which is connected by the path of the selected path point is searched by selecting a connection terminal of a resistor based on the resistor rule.

[Para 14]   According to an embodiment of the present invention, the method of finding paths in IP component further comprises: analyzing the type of all I/O ports in the IP component; and comparing each I/O port of the IP component with the I/O port information provided by the database. Wherein, the I/O port can be an input port, an output port or a bi-directional port. In addition, the method further comprises the step of excluding any path, which

is input/output from any I/O port in the IP component and do not pass through any circuitry in the IP component.

[Para 15]   The present invention is also directed to a computer readable recording media for storing a program implemented by a computer system, and the program comprises following instructions: reading an IP component; automatically generating a plurality of test patterns for all paths in the IP component; sequentially reading each of the test patterns for performing simulation on the IP component and generating a plurality of corresponding simulation results; and generating an IP characteristic library based on the simulation results.

[Para 16]   Since the present invention can find all paths in the IP component automatically, a complete set of the test pattern can be determined for all paths, and simulation results for all paths can be further obtained, such that a complete IP characteristic library can be generated automatically. Since the IP characteristic library is automatically generated without any manual operation, not only a complete IP characteristic library for all paths can be generated, but also the time required for generating it is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 17]   The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

[Para 18]   FIG. 1 is a flow chart illustrating a method of IP characterization according to an embodiment of the present invention.

[Para 19]   FIG. 2 is a flow chart illustrating a method of finding paths in IP component according to an embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[Para 20]　FIG. 1 is a flow chart illustrating a method of IP characterization according to an embodiment of the present invention. Referring to FIG. 1, first, an IP component is provided and analyzed (step S110). Next, a plurality of corresponding test patterns for all paths in the IP component is automatically generated (step S120). Next, the test pattern generated (at step S120) is sequentially fed into the IP component for simulation to generate a plurality of corresponding simulation results (step S130). Finally, an IP characteristic library is generated based on the simulation results (step S140).

[Para 21]　According to an embodiment of the present embodiment, the IP characteristic library mentioned above comprises the timing information and power information corresponding to each of the test patterns. Wherein, the IP component mentioned above is, for example, configured by a Hardware Description Language (HDL).

[Para 22]　According to an embodiment of the present embodiment, step S120 comprises step S122 and step S124. At step S122, all paths in the IP component are searched automatically. Next, the process proceeds to step S124, in which the corresponding test bench for each path is generated.

[Para 23]　Here, step S122 may be implemented with reference to FIG. 2. FIG. 2 is a flow chart illustrating a method of finding paths in IP component according to an embodiment of the present invention. In such method, a breadth-first recursive algorithm is used to find all paths in the IP component, and the IP component is analyzed (step S210). In the present embodiment, since step S210 is the same as step S110, step S210 is omitted herein.

[Para 24]　At step S212, the type of all I/O ports in the IP component is analyzed against a database. Wherein, the I/O port can be an input port, an output port, or a bi-directional port. Then, the process goes to step S214, in which the I/O port of the IP component is compared with the I/O port information stored in the database. Then in step S216, the path, which is input/output to/from any I/O port in the IP component and not passed through any circuitry in the IP component is excluded so as to prevent the bi-directional port from feeding through itself.

[Para 25]   Next, an ESD path is identified and excluded (step S220). Since the ESD protection circuitry does not provide any function when it is normally operated, it is not required to search the ESD path. It is required for the ESD protection circuitry to lead in a great amount of current, thus the width of the ESD protection circuitry is rather wider. By using this characteristic, the ESD path can be easily identified and excluded.

[Para 26]   Next, at step S230, whether there is a path point which has not been completely searched is determined. If all path points are searched, the step of finding all paths in the IP component is completed in step S280. Otherwise, the process proceeds to step S240, in which the path finding is performed on one of the path points, which had not been completely searched.

[Para 27]   Next, at step S250, whether the path point currently found is an end point of this path is determined (here, whether it is the end point of this path or not is easily determined by configuring the end point of the IP component as VCC or GND in advance). If it is determined that the path point currently found is an end point of the path, the path finding of this path is completed, whether there is a path point which has not been completely searched is determined (step S230). If it is determined that the path point currently found is not the end point of the path, a next path point is then searched by selecting a connection terminal of the current path point based on the transistor rule (step S260) and based on the resistor rule (step S270). For example, if the tracked path is electrically coupled to a source of a MOS transistor (path point), it is known from the transistor rule that the signal input from the source cannot be output from the gate of the transistor, thus a drain of the MOS transistor is selected for tracking a next path point. Here, the breadth-first recursive algorithm is repeatedly used to perform the steps of S250~S270 until the path finding is totally completed.

[Para 28]   Referring to FIG. 1, step S140, for example, comprises step S142 and step S144. In step S142, key data is extracted from each of the simulation results, respectively. In the present embodiment, for example, the timing information (e.g. delay time) and the power consumption information for present simulation are extracted from each of the simulation results. At step

S144, the key data of each of the simulation results is integrated to generate a complete IP characteristic library.

[Para 29]   Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.